Remarks:

Applicants appreciatively acknowledge the Examiner's confirmation of receipt of Applicants' claim for priority and certified priority document under 35 U.S.C. § 119(a)-(d).

Reconsideration of the application, as amended herein, is respectfully requested.

Claims 1 - 8 are presently pending in the application. Claims 1 and 3 - 8 have been amended. Claims 9 - 14 have been canceled.

In item 4 of the above-identified Office Action, claims 1 - 14 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 6,762,967 to Tanizaki ("**TANIZAKI**") in view of U. S. Patent No. 5,299,168 to Kang ("**KANG**").

Applicants respectfully traverse the above rejections, as applied to the amended claims.

As background, Applicants' claimed invention recites a particular method for checking the refresh function of a memory having a refresh device. As such, Applicants' claimed invention does **not** test **the information memory**, itself, but rather, checks one of **the refresh devices** executing the

refresh functions of the information memory. For this check, **an external counter** (Cnt_{ext} of Applicants' figure) and **an external oscillator** (Ocs_{ext} of Applicants' figure) are used, which, **by means of a multiplexer** (MUX of Applicants' figure), supply the control unit (CTRL of Applicants' figure) of the information memory (MEM of Applicants' figure) in a test operation **with refresh test pulses** (Rtest of Applicants' figure) **instead of normal refresh request pulses** (Ref of Applicants' figure). In this case, **the multiplexer MUX is controlled by a test signal** (Test of Applicants' figure).

In accordance with the above, Applicants' claim 1 has been amended to recite, among other limitations:

> **supplying refresh test pulses produced outside the memory using a freely cycling external oscillator and an external counter to a control unit of the memory via a multiplex device**, the refresh test pulses being supplied to the control unit **instead of supplying the control unit with the refresh request pulses, the multiplex device being controlled by a test signal**; [emphasis added by Applicants]

As such, Applicants' invention requires, among other things, **providing refresh test pulses, produced outside the memory using a freely cycling external oscillator and an external counter, to the control unit of the memory via a multiplex device that is controlled by a test signal.** Applicants' claimed method additionally requires determining whether and at what intervals refresh request pulses (Ref of Applicants'

figure) are generated on the information memory by detecting these refresh request pulses on a pad (pd of Applicants' figure). As discussed above, Applicants' claimed invention requires that, dependent upon a test signal controlling the multiplexer MUX, refresh test pulses RTest from the external oscillator Osc_{ext} and the external counter Cnt_{ext} are supplied, to the control unit CTRL. Applicants' claims further require, among other things, checking the refresh device of the memory MEM utilizing the refresh test pulses RTest. Resultantly, in the method of the present invention, the memory refresh device is checked using refresh test pulses RTest generated external to (i.e., "outside") the memory.

Applicants' claimed invention is neither taught, nor suggested, by the combination of the **TANIZAKI** and **KANG** references. More particularly, among other limitations of Applicants' amended claim 1, the **TANIZAKI** and **KANG** references fail to teach or suggest **checking a refresh device**, as particularly claimed by Applicants'.

Rather, **TANIZAKI** discloses a semiconductor memory device having a circuit for fast operation. Col. 2 of **TANIZAKI**, lines 5 - 11, state:

> Preferably, the control circuit includes a refresh circuit issuing an automatic refresh signal for executing a refreshing operation of the memory cell

> array. **The refresh circuit operates in a normal operation to issue the automatic refresh signal in response to an external command, and operates in the test mode to issue the automatic refresh signal in synchronization with the output of the clock buffer.** [emphasis added by Applicants]

As such, **TANIZAKI** discloses that in "test mode", a refresh device in the memory operates to issue an automatic refresh signal in synchronization with the output of the clock buffer. The automatic refresh signal of the "test mode" described in **TANIZAKI** is used to execute a "disturb test", as disclosed in col. 2 of **TANIZAKI**, lines 47 - 48. A "disturb test" is defined in Col. 1 of **TANIZAKI**, lines 17 - 23, which state:

> **A disturb test is a kind of known test for semiconductor memory devices.** In the disturb test, a series of operations is performed as follows. A word line is raised to read out data in a memory cell onto a bit line. The data thus read is amplified by a sense amplifier, and is rewritten into the memory cell, and the word line is lowered. **By the above operations, a memory cell on a neighboring unselected word line is disturbed.** [emphasis added by Applicants]

As such, the automatic refresh signal issued in the test mode of **TANIZAKI** is **not used to test the refresh device**, as required by Applicants' claims, but rather, **is used to test the semiconductor memory device** of **TANIZAKI**. **TANIZAKI** fails to teach or suggest any kind of check or test **of the refresh device of an information memory**, as required by Applicants' claims. Additionally, as acknowledged on page 3 of the Office Action, **TANIZAKI** also fails to teach or suggest "determining

if refresh request pulses are being produced on the memory and at what intervals of time the refresh request pulses are being produced on the memory", among other limitations of Applicants' claims.

Instead, page 3 of the Office Action alleges that the **KANG** reference discloses "the complete cycle of addresses based on refresh pulses is verified as well as the 'cycle time' of the refrech cycle (column 5, lines 58-64)". Applicants respectfully disagree that the combination of **TANIZAKI** and **KANG** teach or suggest all limitations of Applicants' amended claim 1.

Rather, the **KANG** reference discloses **a circuit for detecting refresh address signals** of a semiconductor memory device, in order to check **whether all internal refresh addresses** have been generated for a complete refresh cycle. This can be seen from Col. 2 of **KANG**, lines 26 - 30, which state:

> It is still another object of the present invention to provide a semiconductor memory device capable of determining **whether all internal refresh addresses corresponding to a complete self-refresh cycle are completely generated.** [emphasis added by Applicants]

KANG discloses that, for this purpose, the path of an address signal is divided into individual sub-paths for which the addresses are checked individually by means of comparison.

See, for example, Col. 2 of KANG, lines 31 - 49. Thus, KANG discloses checking individual refresh request pulses (i.e., for the refreshing of individual addresses). However, KANG **fails** to teach suggest or motivate in any way, **detecting refresh request pulses from a separate pad (pd)**, and then, **supplying externally generated refresh test pulses, via a multiplexer, to check the operation of the refresh device.**

As such, neither **TANIZAKI**, nor **KANG**, teach or suggest, among other limitations of Applicants' claims, **detecting refresh request signals at a pad, but checking the refresh device using refresh test pulses produced outside the memory** (i.e., using a freely cycling external oscillator and an external counter), **which refresh test pulses are provided to the control unit of the memory via a multiplex device controlled by a test signal instead of the refresh request signals.**

For the foregoing reasons, among others, Applicants' claims are believed to be patentable over the **TANIZAKI** and **KANG** references.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art. The dependent claims are believed

to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1 - 14 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

For Applicants

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